ZT2083

I²C Resistive Touch Screen Controller

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Rev. 0.6
Sep. 11, 2008

■ This data sheet is subject to change without notice.

REVISION HISTORY

Rev.	Date
0.5	08.07.29
0.6	08.09.11

FEATURES

- 4-wire resistive touch screen controller
- SAR ADC resolution: 12 bits
- I^2C interface supports:
  Standard Mode, Fast Mode
- 2.5V to 5.25V operation
- Touch pressure measurement
- Auto power down
- MSOP-10L package
- RoHS Compliant and 100% Lead (Pb) Free

APPLICATIONS

- Cellular phones
- Personal digital assistants
- Portable instruments
- Touch screen monitors

ORDERING INFORMATION

PART	PACKAGE	RoHS	Ship, Quantity
ZT2083	MSOP-10L	Yes	Tape and Reel

DESCRIPTION

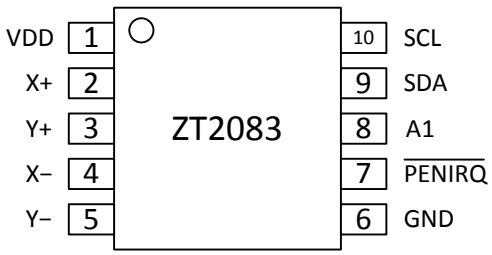
The ZT2083 is a 4-wire resistive touch screen controller with I^2C interface. The resolution is 12 bits. The I^2C interface supports the standard mode 100kHz and the fast mode 400kHz. The ZT2083 can also measure touch pressure.

The ZT2083 powers down the SAR ADC automatically at the end of data conversion when the $\overline{\text{PENIRQ}}$ is enabled.

The ZT2083 is available in the MSOP-10L package, and it is RoHS compliant and 100% lead (Pb) free.

Pins Configuration

MSOP-10L Top View



Absolute Maximum Rating

VDD to GND ..... –0.3V to +6V
Input Voltage to GND ..... –0.3V to +VDD+0.3V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature (T_J Max) ..... +150°C
Lead Temperature, Soldering ..... +260°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

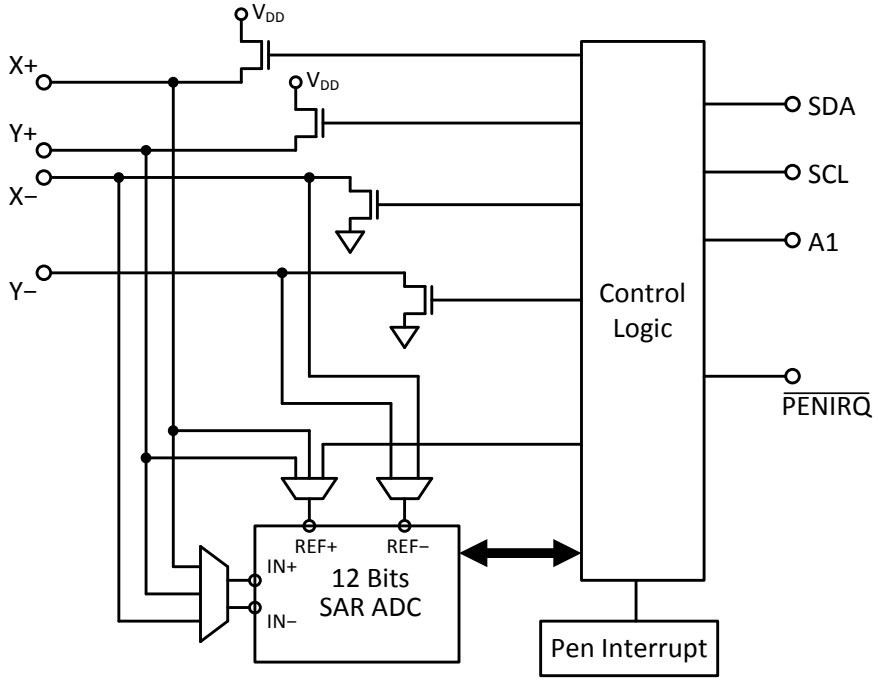
Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

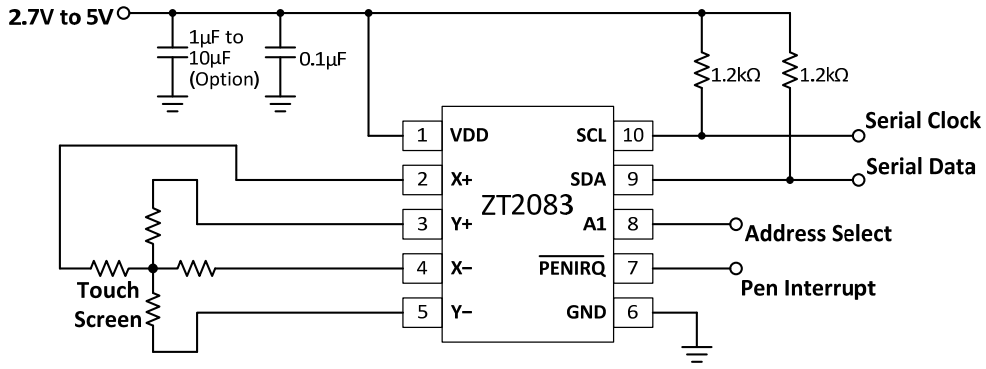
Pins Description

Pin	Symbol	Description
1	VDD	Power Supply.
2	X+	X+ Position Input.
3	Y+	Y+ Position Input.
4	X–	X– Position Input.
5	Y–	Y– Position Input.
6	GND	Ground.
7	$\overline{\text{PENIRQ}}$	Pen Interrupt Output.
8	A1	I^2C Bus Slave Address Input Bit A1.
9	SDA	I^2C Serial Data.
10	SCL	I^2C Serial Clock.

Block Diagram



Basic Application Circuit



Electrical Specifications

(T_A = −40°C to +85°C, $+V_{DD}$ = +2.7V, 12-bit mode and digital inputs = GND or $+V_{DD}$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Full-Scale Input Span		0		V_{REF}	V
Absolute Input Range		–0.2		$+V_{DD}$+0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes	Standard and Fast Mode	11			Bits
Integral Linearity Error	Standard and Fast Mode			±2	LSB(1)
Offset Error				±6	LSB(1)
Gain Error				±4	LSB(1)
SAMPLING DYNAMICS					
Throughput Rate			8.2		Ksps
SWITCH DRIVERS					
On-Resistance					
Y+, X+			5.5		Ω
Y–, X–			7.3		Ω
Drive Current(2)	Duration 100ms			50	mA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels, Except $\overline{PENIRQ}$					
V_{IH}	$\lvert I_{IH} \rvert \le +5\mu A$	$+V_{DD} \bullet 0.7$		$+V_{DD} + 0.3$	V
V_{IL}	$\lvert I_{IL} \rvert \le +5\mu A$	–0.3		$+V_{DD} \bullet 0.3$	V
V_{OH}	$I_{OH} = -250\mu A$	$+V_{DD} \bullet 0.8$			V
V_{OL}	$I_{OL} = 250\mu A$			0.4	V
$\overline{PENIRQ}$ V_{OL}	30kΩ Pull-Up			0.4	V
Data Format			Straight Binary		
Input Capacitance	SDA, SCL Lines			10	pF
POWER-SUPPLY REQUIREMENTS					
+VDD	Specified Performance	2.7		3.6	V
	Operating Range	2.5		5.25	V
Quiescent Current	PD1 = PD0 = 0				
	Fast Mode: SCL = 400kHz		95		µA
	Standard Mode: SCL = 100kHz		63		µA
Power-Down Current when Part is	PD1 = PD0 = 0				
Not Addressed	Fast Mode: SCL = 400kHz		21		µA
	Standard Mode: SCL = 100kHz		4		µA
	PD1 = PD0 = 0, SDA = SCL = $+V_{DD}$			3	µA
Power Dissipation	$+V_{DD}$ = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		−40		+85	°C

NOTES:

(1) LSB means Least Significant Bit.

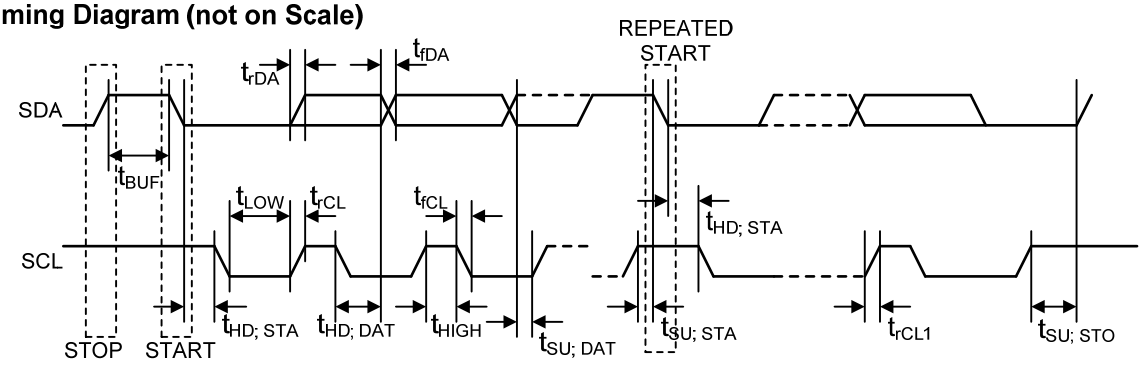
(2) Ensured by design, but not tested. Exceeding 50mA source current may result in device degradation.

Timing Specifications

(T_A = −40°C to +85°C, $+V_{DD}$ = +2.7V, unless otherwise noted. All values referred to V_{IHMIN} and V_{ILMAX} levels.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard Mode Fast Mode	0 0	100 400	kHz kHz
Bus Free Time Between a STOP and Start Condition	t_{BUF}	Standard Mode Fast Mode	4.7 1.3		µs µs
Hold Time (Repeated) START Condition	$t_{HD;\ STA}$	Standard Mode Fast Mode	4.0 600		µs ns
LOW Period of the SCL Clock	t_{LOW}	Standard Mode Fast Mode	4.7 1.3		µs µs
HIGH Period of the SCL Clock	t_{HIGH}	Standard Mode Fast Mode	4.0 600		µs ns
Setup Time for a Repeated START Condition	$t_{SU;\ STA}$	Standard Mode Fast Mode	4.7 600		µs ns
Data Setup Time	$t_{SU;\ DAT}$	Standard Mode Fast Mode	250 100		ns ns
Data Hold Time	$t_{HD;\ DAT}$	Standard Mode Fast Mode	0 0	3.45 0.9	µs µs
Rise Time of SCL Signal	t_{rCL}	Standard Mode Fast Mode	 $20 + 0.1C_b$	1000 300	ns ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	t_{rCL1}	Standard Mode Fast Mode	 $20 + 0.1C_b$	1000 300	ns ns
Fall Time of SCL Signal	t_{fCL}	Standard Mode Fast Mode	 $20 + 0.1C_b$	300 300	ns ns
Rise Time of SDA Signal	t_{rDA}	Standard Mode Fast Mode	 $20 + 0.1C_b$	1000 300	ns ns
Fall Time of SDA Signal	t_{fDA}	Standard Mode Fast Mode	 $20 + 0.1C_b$	300 300	ns ns
Setup Time for STOP Condition	$t_{SU;\ STO}$	Standard Mode Fast Mode	4.0 600		µs ns
Capacitive Load for SDA or SCL Line	C_b	Standard Mode Fast Mode		400 400	pF pF
Pulse Width of Spike Suppressed	t_{SP}	Fast Mode	0	50	ns
Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	V_{nH}	Standard Mode Fast Mode	$0.2V_{DD}$		V
Noise Margin at LOW Level for Each Connected Device (Including Hysteresis)	V_{nL}	Standard Mode Fast Mode	$0.1V_{DD}$		V

Timing Diagram (not on Scale)



FUNCTIONAL DESCRIPTION

Overview

The ZT2083 is a classic Successive Approximation Register (SAR) Analog-to-Digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function.
The device features an internal clock. Operation is maintained from a single supply of 2.7V to 5.25V.
The analog input (X, Y, and Z parallel coordinates) to the converter is provided via a multiplexer. A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power, and an accompanying pin to provide ground for an external device. By maintaining a differential input to the converter, and a differential reference architecture, it is possible to negate the switch's on-resistance error (should this be a source of error for the particular measurement).

Analog Input

See block diagram of the ZT2083, the input multiplexer, the differential input of the A/D converter, and the converter's differential reference.
When the converter enters the Hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

Differential Mode

See Figure 1, by using the differential mode, the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This makes the A/D converter ratiometric. The result of the conversion is always a percentage of the external reference, regardless of how it changes in relation to the on-resistance of the internal switches.
Differential reference mode always uses the supply voltage, through the drivers, as the reference voltage for the A/D converter.

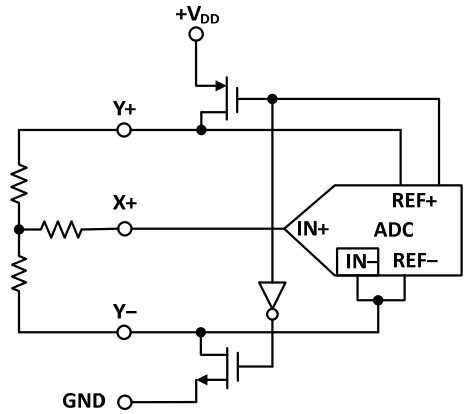


Figure 1: Simplified diagram of differential reference (Y switches enabled, X+ is analog input).

Touch Screen Settling

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (i.e., noise generated by the LCD panel or backlight circuitry). These capacitors will provide a low-pass filter to reduce the noise, but they will also cause a settling time requirement when the panel is touched. The settling time will typically show up as a gain error. The problem is that the input and/or reference has not settled to its final steady-state value prior to the A/D converter sampling the input(s), and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle.
To resolve these settling time problems, the ZT2083 can be commanded to turn on the drivers only without performing a conversion (see Table 1). Time can then be allowed before the command is issued to perform a conversion. Generally, the time it takes to communicate the conversion command over the I^2C bus is adequate for the touch screen to settle.

Pressure Measurement

Measuring touch pressure can also be done with the ZT2083. To determine pen or finger touch, the pressure of the "touch" needs to be determined. Generally, it is not necessary to have high accuracy for this test, therefore, the 8-bit resolution mode is recommended. However, calculations will be shown with the 12-bit resolution mode. There are several different ways of performing this measurement, the ZT2083 supports two methods.

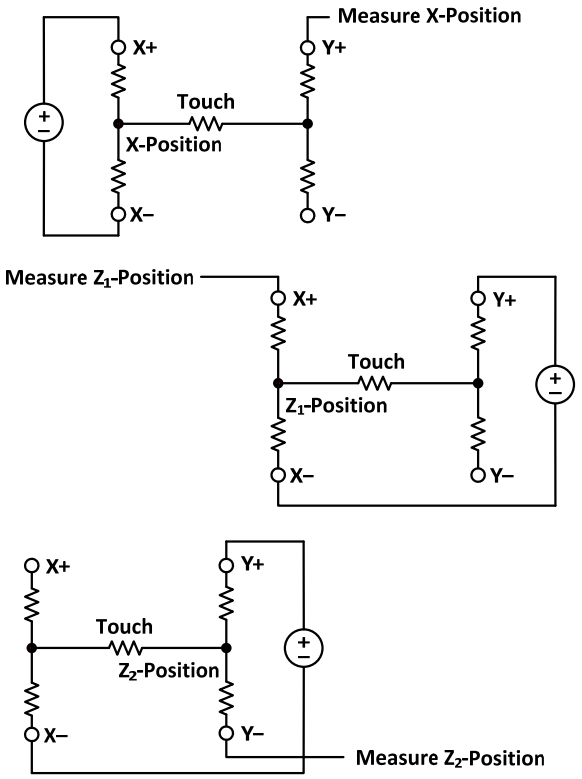


Figure 2: Pressure measurement block diagrams.

The first method requires knowing the X-Plate resistance, measurement of the X-Position, and two additional cross-panel measurements (Z_2 and Z_1) of the touch screen, as shown in Figure 2. Using Equation 1 will calculate the touch resistance:

$$R_{Touch} = R_{X\text{-}Plate} \times \frac{X\text{-}Position}{4096} \times \left(\frac{Z_2}{Z_1} - 1\right) \quad (1)$$

The second method requires knowing both the X-Plate and Y-Plate resistance, measurement of X-Position and Y-Position, and Z_1. Equation 2 calculates the touch resistance using the second method:

$$R_{Touch} = R_{X\text{-}Plate} \times \frac{X\text{-}Position}{4096} \times \left(\frac{4096}{Z_1} - 1\right) - R_{Y\text{-}Plate} \times \left(1 - \frac{Y\text{-}Position}{4096}\right) \quad (2)$$

Digital Interface

The ZT2083 supports the I^2C serial bus and data transmission protocol in two defined modes: standard and fast modes. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The ZT2083 operates as a slave on the I^2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SDL.

The following bus protocol has been defined, as shown in Figure 3:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH defines a STOP condition.

Data Valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise, and each receiver acknowledges with a ninth-bit.

Within the I^2C bus specifications, a standard mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The ZT2083 works in the two modes.

Acknowledge: Each receiving device, when accessed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 3 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

- **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last one. At the end of the last received byte, a 'not acknowledge' is returned.

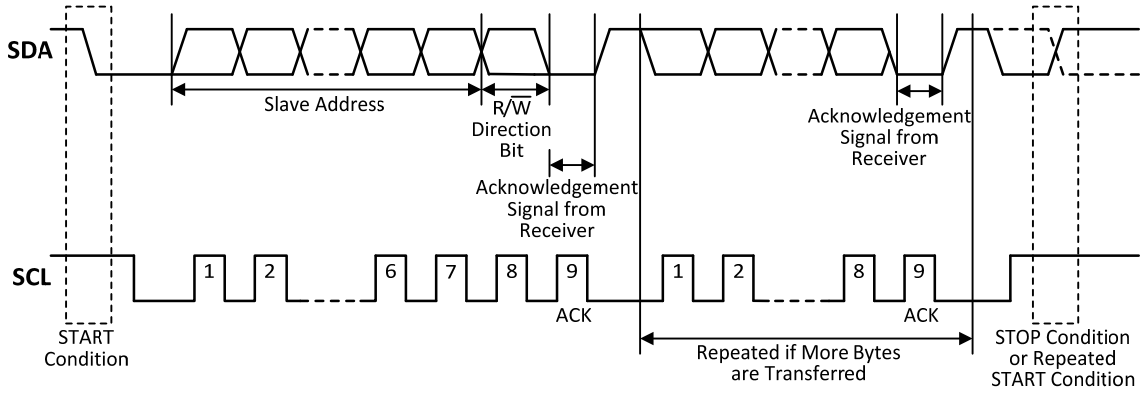


Figure 3: I²C bus protocol.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The ZT2083 may operate in the following two modes:

- **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode:** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ZT2083 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Address Byte

The address byte, as shown in Figure 4, is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory preset to 10010. The next bit of the address byte is the device select bit: A1. The seventh bit is factory preset to 0. Input pin A1 on the ZT2083 determines the bit of the device address for a particular ZT2083. Therefore, a maximum of two devices with the same preset code can be connected on the same bus at one time.

MSB							LSB
1	0	0	1	0	A1	0	R/$\overline{W}$

Figure 4: Address byte.

The A1 Address Input can be connected to V_{DD} or digital ground. The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a "1", a read operation is selected; when set to a "0", a write operation is selected. Following the START condition, the ZT2083 monitors the SDA bus and checks the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bit, the 0 code, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The ZT2083's operating mode is determined by a command byte, which is shown in Figure 5.

MSB							LSB
C3	C2	C1	C0	PD1	PD0	M	X

Figure 5: Command byte.

The bits in the device command byte are defined as Table 1.

- **C3-C0:** Configuration bits. These bits set the input multiplexer address and functions that the ZT2083 will perform, as shown in Table 1.

C3	C2	C1	C0	Function	Input to ADC	X-Drivers	Y-Drivers	Reference Mode
0	1	1	1	Refer to Table 3	----	----	----	----
1	0	0	0	Activate X+, X− Drivers	----	ON	OFF	Differential
1	0	0	1	Activate Y+, Y− Drivers	----	OFF	ON	Differential
1	0	1	0	Activate Y+, X− Drivers	----	X− ON	Y+ ON	Differential
1	0	1	1	Reserved	----	----	----	Differential
1	1	0	0	Measure X position	Y+	ON	OFF	Differential
1	1	0	1	Measure Y Position	X+	OFF	ON	Differential
1	1	1	0	Measure Z_1 Position	X+	X− ON	Y+ ON	Differential
1	1	1	1	Measure Z_2 Position	Y−	X− ON	Y+ ON	Differential

Table 1: Possible input configurations.

- **PD1-PD0:** Power-down bits. These two bits select the power down mode that the ZT2083 will be in after the current command completes, as shown in Table 2.

PD1	PD0	$\overline{\text{PENIRQ}}$	Description
0	0	Enabled	Power-Down between conversions
0	1	Enabled	Analog-to-Digital Converter ON
1	0	Enabled	Analog-to-Digital Converter OFF
1	1	Disabled	Analog-to-Digital Converter ON

Table 2: Power-down bits function.

It is recommended to set PD0 = 0 in each command byte to get the lowest power consumption possible. If multiple X-, Y-, and Z-position measurements will be done one right after another, such as when averaging, PD0 = 1 will leave the touch screen drivers on at the end of each conversion cycle.

- **M**: Mode bit. If M is 0, the ZT2083 is in 12-bit mode. If M is 1, 8-bit mode is selected.
- **X:** Don't care.

When the ZT2083 powers up, the power-down mode bits need to be written to ensure that the part is placed into the desired mode to achieve lowest power.

Therefore, immediately after power-up, a command byte should be sent which sets PD1 = PD0 = 0, so that the device will be in the lowest power mode, powering down between conversions.

Start a Conversion/Write Cycle

A Conversion/Write Cycle begins when the master issues the address byte containing the slave address of the ZT2083, with the eighth bit equal to a 0 (R/$\overline{\text{W}}$ = 0), as shown in Figure 4. Once the eighth bit has been received, and the address matches the A1 address input pin setting, the ZT2083 issues an acknowledge.

Once the master receives the acknowledge bit from the ZT2083, the master writes the command byte to the slave (see Figure 5). After the command byte is received by the slave, the slave issues another acknowledge bit. The master then ends the Write Cycle by issuing a repeated START or a STOP condition, as shown in Figure 6.

If the master sends additional command bytes after the initial byte, before sending a STOP or repeated START condition, the ZT2083 will not acknowledge those bytes.

The input multiplexer for the A/D converter has its channel selected when bits C3 through C0 are clocked in. If the selected channel is an X-, Y-, or Z-position measurement, the appropriate drivers will turn on once the acquisition period begins.

When R/$\overline{\text{W}}$ = 0, the input sample acquisition period starts on the falling edge of SCL once the C0 bit of the command byte has been latched, and ends when a STOP or repeated START condition has been issued. A/D conversion starts immediately after the acquisition period. The multiplexer inputs to the A/D converter are disabled once the conversion period starts. However, if an X-, Y-, or Z-position is being measured, the respective touch screen drivers remain on during the conversion period. A complete Write Cycle is shown in Figure 6.

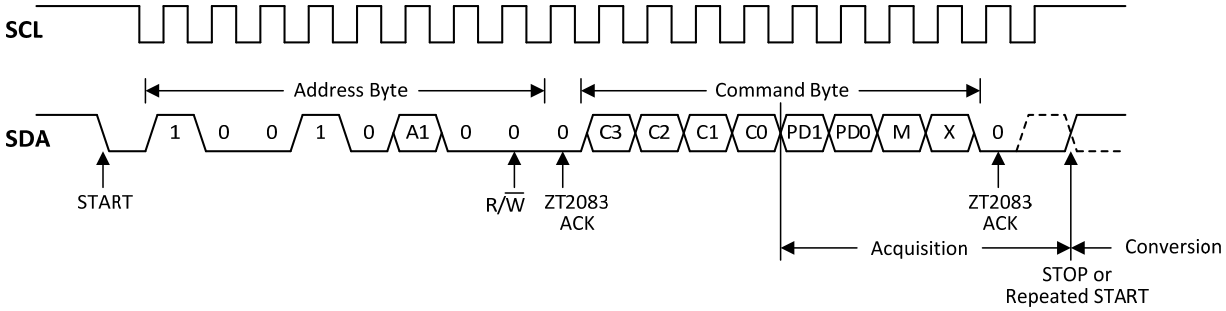


Figure 6: Complete I^2C serial write transmission.

Read a Conversion/Read Cycle

For best performance, the I^2C bus should remain in an idle state while an A/D conversion is taking place. This prevents digital clock noise from affecting the bit decisions being made by the ZT2083. The master should wait for at least 10μs before attempting to read data from the ZT2083 to realize this best performance. However, the master does not need to wait for a completed conversion before beginning a read from the slave, if full 12-bit performance is not necessary.

Data access begins with the master issuing a START condition followed by the address byte (see Figure 4) with R/$\overline{W}$ = 1. Once the eighth bit has been received, and the address matches, the slave issues an acknowledge. The first byte of serial data will follow (D11-D4, MSB first).

After the first byte has been sent by the slave, it releases the SDA line for the master to issue an acknowledge. The slave responds with the second byte of serial data upon receiving the acknowledge from the master (D3-D0, followed by four 0 bits). The second byte is followed by a NOT acknowledge bit (ACK = 1) from the master to indicate that the last data byte has been received. If the master acknowledges the second data byte, then the data will repeat on subsequent reads with ACKs between bytes. This is true in both 12-bit and 8-bit mode. The master will then issue a STOP condition, which ends the Read Cycle, as shown in Figure 7.

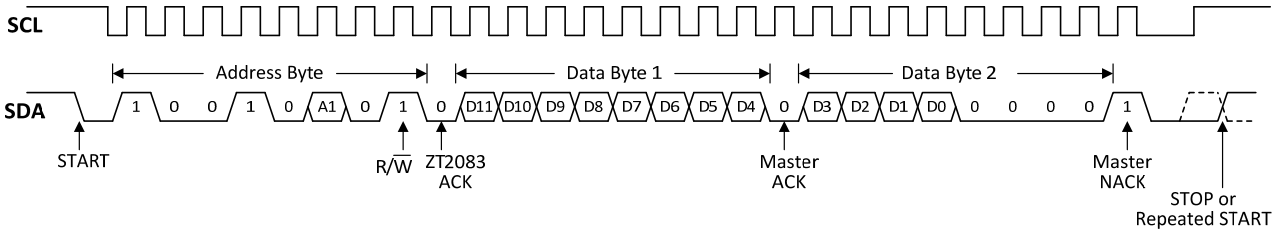
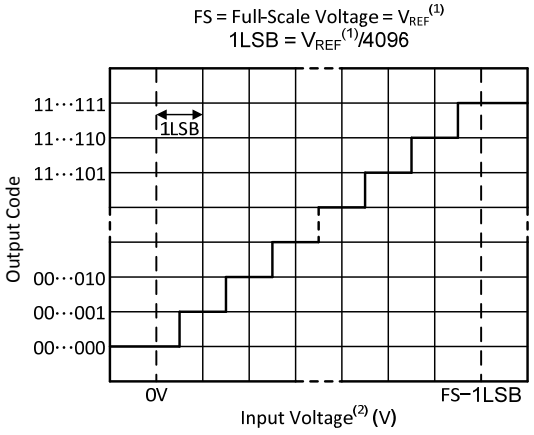


Figure 7: Complete I^2C serial read transmission.

Data Format

The ZT2083 output data is in Straight Binary format, as shown in Figure 8. This shows the ideal output code for the given input voltage, and does not include the effects of offset, gain, or noise.



Notes:
(1) Reference voltage at converter: +REF − (−REF). See Figure 1.
(2) Input voltage at converter, after multiplexer: +IN − (−IN). See Figure 1.

Figure 8: Ideal input voltages and output codes.

8-Bit Conversion

The ZT2083 provides an 8-bit conversion mode (M = 1) that can be used when faster throughput is needed, and the digital result is not as critical (for example, measuring pressure). By switching to the 8-bit mode, a conversion result can be read by transferring only one data byte.

This shortens each conversion by four bits and reduces data transfer time which results in fewer clock cycles and provides lower power consumption.

Sleep Mode

ZT2083 supports a sleep mode to put touch screen interface into open state and disable pen interrupt function. ZT2083 will get into sleep mode when the master writes the command byte to ZT2083 as shown in Table 3. The output state of $\overline{\text{PENIRQ}}$ pin in sleep mode depends on the mode bit, and the touch panel interface states (Y+, Y−, X+, X−) are open. ZT2083 keeps in sleep mode until the next enable command byte is received.

Command	Mode Bit	$\overline{\text{PENIRQ}}$	Touch Panel Interface
0111X01X	M = 1	High-Z	Open
0111X00X	M = 0	Output High	Open

Table 3: Sleep mode command.

$\overline{\text{PENIRQ}}$ Output

The pen-interrupt output function is shown in Figure 9. While in the power-down mode, with PD0 = 0, the Y–

driver is ON and connected to GND, and the $\overline{\text{PENIRQ}}$ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and $\overline{\text{PENIRQ}}$ output goes LOW due to the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input will be disconnected from the $\overline{\text{PENIRQ}}$ pull-down transistor to eliminate any leakage current from the pull-up resistor to flow through the touch screen, thus causing no errors.

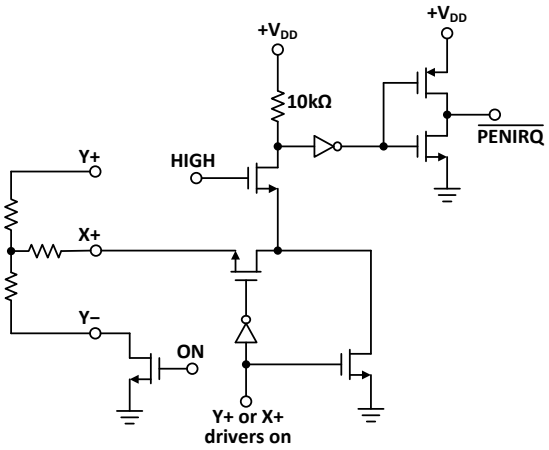


Figure 9: $\overline{\text{PENIRQ}}$ functional block diagram.

In addition to the measurement cycles for X-, Y-, and Z-position, commands which activate the X drivers, Y drivers, Y+ and X− drivers without performing a measurement also disconnect the X+ input from the $\overline{\text{PENIRQ}}$ pull-down transistor and disable the pen-interrupt output function regardless of the value of the PD0 bit. Under these conditions, the $\overline{\text{PENIRQ}}$ output will be forced LOW. Furthermore, if the last command byte written to the ZT2083 contains PD1 = PD0 = 1, the pen-interrupt output function will be disabled and will not be able to detect when the panel is touched. In order to re-enable the pen-interrupt output function under these circumstances, a command byte needs to be written to the ZT2083 with PD1 = PD0 = 0.

Once the bus master sends the address byte with R/$\overline{\text{W}}$ = 0 (see Figure 4) and the ZT2083 sends an acknowledge, the pen-interrupt function is disabled. If the command which follows the address byte has PD0 = 0, then the pen-interrupt function will be enabled at the end of a conversion. This is approximately 10μs (12-bit mode) or 7μs (8-bit mode) after the ZT2083 receives a STOP/START condition following the reception of a command byte (see Figure 6 for further details of when the conversion cycle begins).

In both cases listed above, it is recommended that the master processor mask the interrupt which the $\overline{\text{PENIRQ}}$ is associated with whenever the host writes to the ZT2083. This will prevent false triggering of interrupts when the $\overline{\text{PENIRQ}}$ line is disabled in the cases listed above.

Layout

The following layout suggestions should provide optimum performance from the ZT2083. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly “clean” power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter's power, and less concern regarding grounding. Still, each situation is unique, and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the ZT2083 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the power supply, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this in mind, power to the ZT2083 should be clean and well bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1μF to 10μF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.

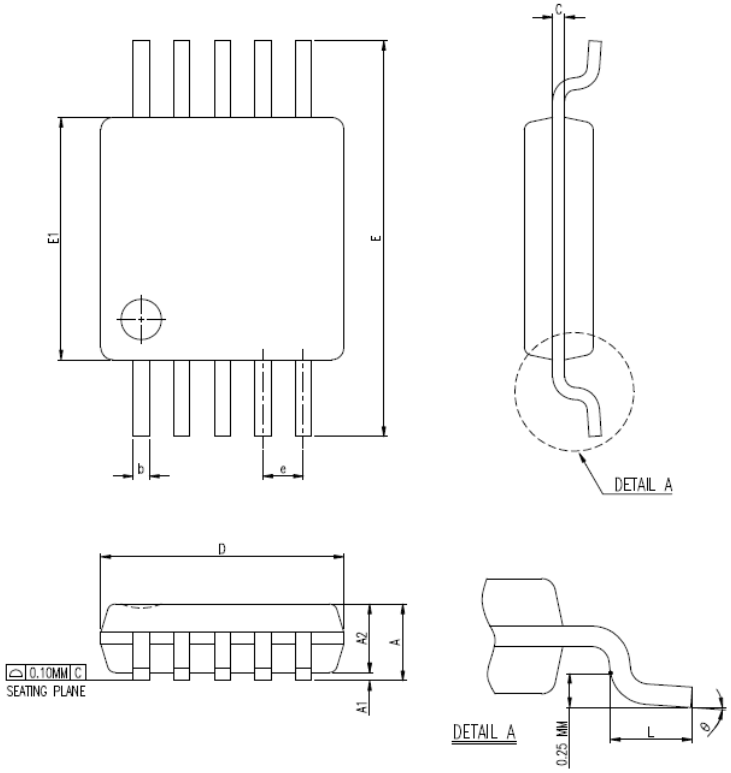
The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the

converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections will be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause “flickering” of the converted data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This will couple the majority of noise to ground. Additionally, filtering capacitors from Y+, Y–, X+, and X– to ground can also help.

PACKAGE DIMENSION (MSOP-10L)



Symbol	Dimension in mm			Dimension in Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.81	1.02	1.10	0.032	0.040	0.043
A1	0.05	---	0.15	0.002	---	0.006
A2	0.75	0.86	0.95	0.030	0.034	0.037
b	0.17	0.20	0.27	0.007	0.008	0.011
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	0.50 Basic			0.020 Basic		
L	0.40	0.55	0.70	0.016	0.022	0.028
θ	0°	3°	6°	0°	3°	6°