

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT151 8-input multiplexer

Product specification
File under Integrated Circuits, IC06

December 1990

8-input multiplexer**74HC/HCT151****FEATURES**

- True and complement outputs
- Multifunction capability
- Permits multiplexing from n lines to 1 line
- Non-inverting data path
- See the "251" for the 3-state version
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT151 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

$GND = 0 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_n to Y, \bar{Y} S_n to Y, \bar{Y} \bar{E} to Y \bar{E} to \bar{Y}	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	17 19 12 14	19 20 13 18	ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION

See "[74HC/HCT/HCU/HCMOS Logic Package Information](#)".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	\bar{Y}	complementary multiplexer output
7	\bar{E}	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0 , S_1 , S_2	select inputs
16	V_{CC}	positive supply voltage

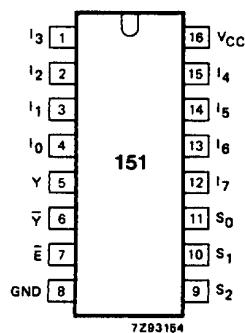


Fig.1 Pin configuration.

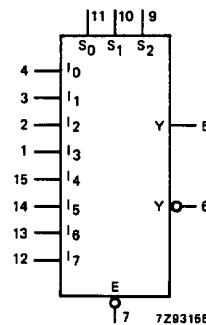


Fig.2 Logic symbol.

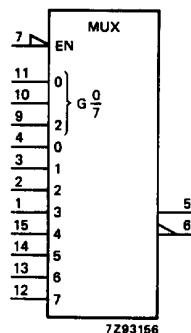


Fig.3 IEC logic symbol.

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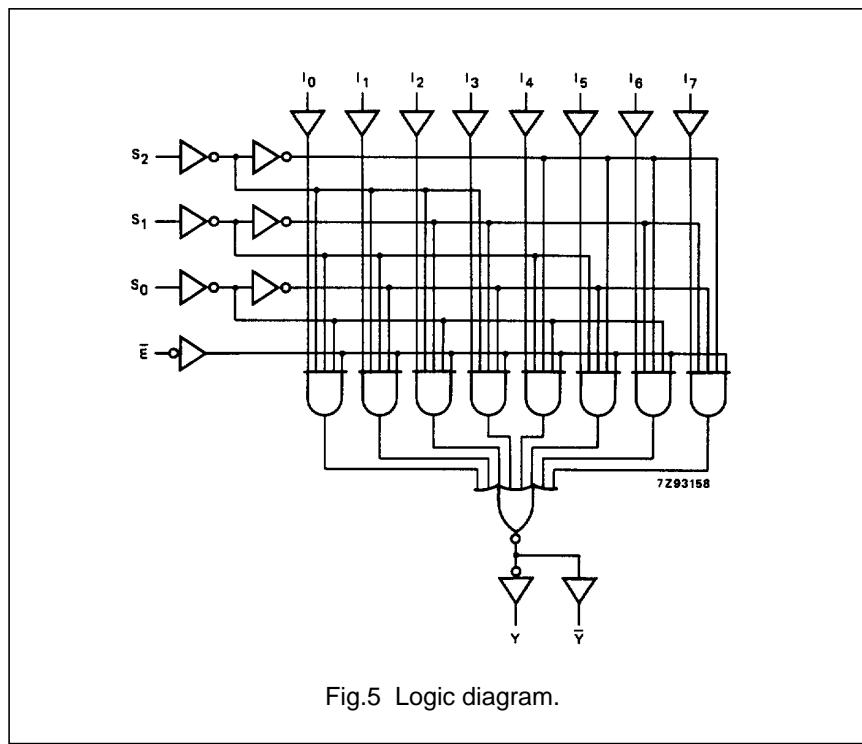
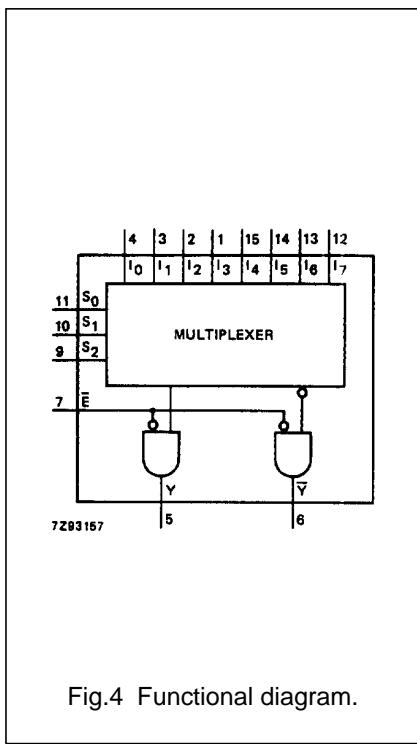
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FUNCTION TABLE

INPUTS													OUTPUTS	
\bar{E}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\bar{Y}	Y	
H	X	X	X	X	X	X	X	X	X	X	X	H	L	
L	L	L	L	L	X	X	X	X	X	X	X	H	L	
L	L	L	L	H	X	X	X	X	X	X	X	L	H	
L	L	L	H	X	L	X	X	X	X	X	X	H	L	
L	L	H	H	X	H	X	X	X	X	X	X	L	H	
L	L	H	H	X	X	X	X	H	X	X	X	L	H	
L	H	L	L	X	X	X	X	L	X	X	X	H	L	
L	H	L	L	X	X	X	X	H	X	X	X	L	H	
L	H	L	H	X	X	X	X	X	L	X	X	H	L	
L	H	H	L	X	X	X	X	X	X	L	X	H	L	
L	H	H	L	X	X	X	X	X	X	H	X	L	H	
L	H	H	H	X	X	X	X	X	X	X	X	H	L	
L	H	H	H	X	X	X	X	X	X	X	X	H	L	

Notes

1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care.



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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

$GND = 0 \text{ V}$; $t_r = t_f = 6 \text{ ns}$; $C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	$T_{amb} (\text{ }^{\circ}\text{C})$						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/ t_{PLH}	propagation delay I_n to Y		52 19 15	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6	
t_{PHL}/ t_{PLH}	propagation delay I_n to \bar{Y}		58 21 17	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.6	
t_{PHL}/ t_{PLH}	propagation delay S_n to Y		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.7	
t_{PHL}/ t_{PLH}	propagation delay S_n to \bar{Y}		61 22 18	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig.7	
t_{PHL}/ t_{PLH}	propagation delay \bar{E} to Y		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.7	
t_{PHL}/ t_{PLH}	propagation delay \bar{E} to \bar{Y}		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7	
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: standard

 I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I_n	0.45
S_n	1.50
\bar{E}	0.30

AC CHARACTERISTICS FOR 74HCT

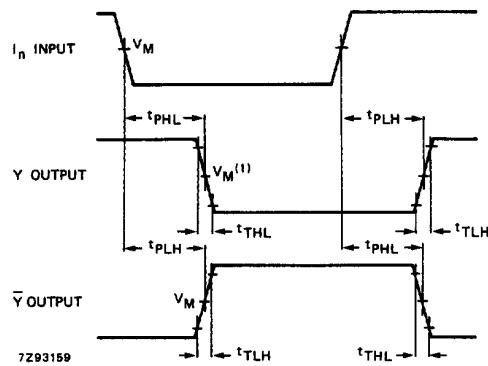
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay I_n to Y		22	38		48		57	ns	4.5	Fig.6	
t_{PHL}/t_{PLH}	propagation delay I_n to \bar{Y}		22	38		48		57	ns	4.5	Fig.6	
t_{PHL}/t_{PLH}	propagation delay S_n to Y		23	41		51		62	ns	4.5	Fig.7	
t_{PHL}/t_{PLH}	propagation delay S_n to \bar{Y}		25	43		54		65	ns	4.5	Fig.7	
t_{PHL}/t_{PLH}	propagation delay \bar{E} to Y		16	29		36		44	ns	4.5	Fig.7	
t_{PHL}/t_{PLH}	propagation delay \bar{E} to \bar{Y}		21	36		45		54	ns	4.5	Fig.7	
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

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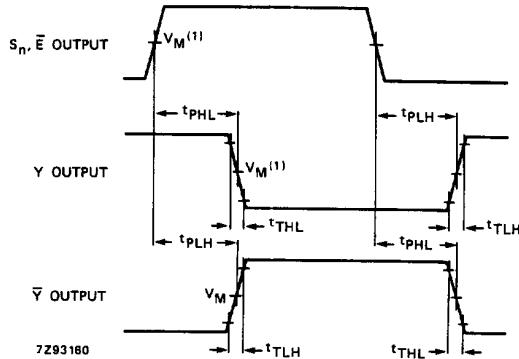
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AC WAVEFORMS



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.6 Waveforms showing the multiplexer input (I_n) to outputs (Y and \bar{Y}) propagation delays and the output transition times.



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the select input (S_n) and enable input (\bar{E}) to outputs (Y and \bar{Y}) propagation delays and the output transition times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".